REMARKS

Drawings

In response to paragraph 4 of the Office action, FIG. 1 has been amended to add labels to elements 28 and 38, FIG. 2 has been amended to add a label to element 40(1), and FIG. 3 has been amended to add labels to elements 50(1), 56, 58, and 60 as requested by the examiner. Replacements sheets have been filed with this response. Annotated sheets showing the changes in red have also been filed.

In response to paragraph 5 of the Office action, applicant reminds the examiner that a replacement FIG. 6 was previously filed on December 22, 2004, which labeled FIG. 6 as "Prior Art." Therefore, it is believed that no further response to paragraph 5 is needed.

Specification

In paragraph 7 of the Office action the abstract was objected to. A revised abstract is submitted herewith which is substantially the same as the abstract suggested by the examiner.

35 U.S.C. § 112, First Paragraph

In paragraph 11 of the Office action, claims 1-38 and 41-44 stand rejected under 35 U.S.C. § 112, first paragraph, for failing to comply with the written description requirement. In paragraph 12 of the Office action, the examiner indicates that the delay circuit is shown in figures 1 and 5, however "nothing more than a blank box or a black box type design is depicted which fails to give any details for one of ordinary skill in the memory arts to make and use a delay circuit in conjunction with a content adjustment memory without undue experimentation" and states that the specification does not provide "sufficient technical details for essential subject matter."

Applicant first notes that nowhere in the specification nor during the prosecution of the instant application has the delay circuit been identified as "essential subject matter."

Second, applicant respectfully reminds the examiner that specifications are written for persons of ordinary skill in the art and preferably omit details that are well known to such persons. *Genetech, Inc. v. Novo Nordisk A/S*, 108 F.3d 1361 (Fed. Cir. 1997).

Third, addressing the merits of the examiner's rejection, it is respectfully submitted that the time required to enable or precharge a content addressable memory would be readily apparent to a person of ordinary skill in the art based on the specifications for the memory such that experimentation would be unnecessary. Knowing the time needed to precharge the memory based on the memory's specifications, those of ordinary skill in the memory art would be easily capable of designing a circuit to provide the necessary delay. For example, when command signals are received in a memory in advance of address signals, it is notoriously well known in the art that the execution of the command signals must be coordinated with the decoding of the address signals. For the examiner to state that a person of ordinary skill in the memory art would not know how to construct a delay circuit based on known precharging times is completely without foundation in the record.

Fourth, the examiner's citation of *Automotive Technologies International, Inc. v. BMS of North America, Inc.*, 501 F.3d 1274 (Fed. Cir. 2007) does not support the examiner's position for at least the following reasons:

- That case involved a situation where a mechanical side impact sensor was disclosed in detail but the claims recited an electronic side impact sensor. There is no dichotomy in the instant application between what is disclosed and what is claimed.

- The court stated that "the novel aspect of this invention is using a velocity-type sensor for side impact sensing." Thus, the specification in the case cited by the examiner was silent precisely at the "point of novelty." The instant applicant has neither in the specification nor during prosecution argued that the delay circuit is novel or that the delay circuit is the "point of novelty."

- The specification in the case cited by the examiner stated that side impact sensing is a new field. There is no corresponding statement in this case that the construction of delay circuits is a new field.

- The court had testimony that indicated that a "great deal of experimentation" would have been necessary to make an electronic side impact sensor after reading the specification in the case cited by the examiner. No such evidence is in the record in the instant application.

Where, as here, the delay circuit has been recited for completeness and not because the delay circuit is the point that distinguishes the clamed subject matter from the prior art, nothing further than a generic description is required. Recitation of "a delay circuit" is analogous to the recitation of "a motor," "an amplifier," or any of hundreds of well known components. Where such components are not the focus of the invention, nothing more than a generic recitation is needed. The rejection under 35 U.S.C. § 112, first paragraph, based on an alleged failure to provide a written description of the delay circuit should be withdrawn.

In paragraph 13, the examiner states the invention is not limited to any particular implementation because of the use of permissive language. The examiner has cited no authority for indicating that the use of permissive (may be) instead of mandatory (is or shall) language is required to meet the written description requirement. The examiner has not shown how the cited case supports the examiner's position, nor has the examiner cited any section of the MPEP, or any controlling authority, indicating that the use of permissive language results in a failure to meet the written description requirement.

Figures are provided in the application which demonstrate to a person of ordinary skill in the art how the circuit is to be implemented. The specification provides a verbal description of the figures. The use of permissive language to leave the door open for the use of substitutes which those of ordinary skill in the art recognize as being equivalent to that which is disclosed in no way indicates that the written description requirement has not been met. The rejection under 35 U.S.C. § 112, first paragraph, based on the use of permissive language should be withdrawn.

Finally, the weakness of the examiner's position is underscored by the fact that this application has been examined numerous times and several Office actions have been issued. At one point, a Notice of Allowance was issued and it is presumed that the instant application underwent a quality review at that time. At no time during this exhaustive examination procedure spanning over two years, was there any hint that the specification was defective for failing to comply with the written description requirement.

For the foregoing reasons, it is respectfully submitted that all objections under 35 U.S.C. § 112, first paragraph, be withdrawn.

Claim Rejections Under 35 U.S.C. § 102(e)

On page 6 of the outstanding Office action, claims 41-44 are rejected under 35 U.S.C. § 102(e) as being anticipated by Cheriton (US 7,002,965).

The portions of Cheriton cited by the Office disclose a TCAM/CAM classifier for classifying and routing data packets. With reference to figure 3, the TCAM/CAM classifier determines the input and output classification for a data packet using a packet buffer (300) that receives data packets from a network, a TCAM (301) that generates a hash index from a full flow label of the data packet (See col. 6, lines 43-47 and 62-65), and a large SRAM (302) that stores a hash directory of data packet classifications for returning a data packet classification based on the hash index (See col. 3, lines 18-21 and col. 6, lines 56-65). The TCAM/CAM classifier determines the routing for the data packet using a mask generator (303) that masks off a portion of the full flow label of the data packet based on the classifications applied to the data packet (See col. 6, lines 66-67 and col. 7, lines 1-2), a hash function (304) that generates a hash index from the masked full flow label (See col. 7, lines 2-7), and a CAM (305) that stores a hash directory of network IP addresses for routing the data packet based on the hash index (See col. 3, lines 18-21 and col. 6, lines 47-49). The TCAM/CAM uses a selection logic circuit (307) to resolve multiple network IP address matches for routing the data packet by using the hash index generated by the TCAM to select a single network IP address match for routing the data packet (See col. 7, lines 12-21).

Applicant respectfully points out that the cited portions of Cheriton do not disclose a method of *initializing* the TCAM/CAM classifier and disclose only methods for classifying and routing data packets. Therefore, the cited portions of Cheriton disclose only the inherent method of initializing the TCAM/CAM classifier to operate to classify and route data packets. The TCAM/CAM classifier disclosed by the cited portions of Cheriton does not have a CAM divided into a plurality of banks and an output memory device responsive to a CAM divided into a plurality of banks. Therefore, the inherent method for initializing the TCAM/CAM classifier will perform a different initialization method from the claimed method because the methods for initializing different hardware are inherently different. To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. See MPEP 2112. Accordingly, it is believed that independent claim 41 as well as dependent claims 42-44 are in condition for allowance.

Claim Rejections Under 35 U.S.C. § 103(a)

On page 7 of the outstanding Office action, claims 1-38 are rejected under 35 U.S.C. § 102(e) as being obvious over Hariguchi et al. (US 6,665,297) in view of Cheriton (US 7,002,965).

The portions of Hariguchi cited by the Office disclose a router for routing datagrams through a network based on the destination address associated with the datagrams. With reference to figure 2A, the router has input ports (42-1 through 42-n) for receiving datagrams from a network, a FIFO buffer (44) for supplying the datagrams to a routing table (40) in a first-in, first-out order. The routing table determines the routing of the datagrams based on the datagrams' destination addresses. The routing table contains hash circuits (82-32 through 82-8) each responsive to one unique prefix of the destination addresses (See col. 5, lines 15-31), a CAM (80) for storing destination addresses to avoid hash collisions in the hash circuits (See col. 6, lines 25-39), a selection stage (88) for selecting an output pointer associated with the longest prefix match (See col. 5, lines 6-14), a pointer register (92) that stores the selected output pointer

(See col. 5, lines 41-45), and a route entry table (98) that stores network addresses (See col. 5, lines 41-44).

When the FIFO buffer provides the routing table with a destination address for a datagram, the hash circuits and the CAM simultaneously receive and determine a network address match for the destination address and then output the output pointers associated with the matching network addresses. The selection stage receives the output pointers and selects the output pointer associated with the longest prefix match for storing in the pointer register. The pointer register provides the route entry table with the selected output pointer and the route entry table outputs the network address for the datagram's next hop based on the selected output pointer. The Office correctly points out on page 9 of the outstanding Office action that Hariguchi, "does not specifically teach using hash signals to enable portions of a CAM." The Office relies on Cheriton to supply the missing teachings.

The portions of Cheriton cited by the Office disclose a TCAM/CAM classifier for classifying and routing data packets. The TCAM/CAM classifier has a CAM (See figure 3, Ref. No. 305) that stores a hash directory of network IP addresses. The CAM performs a comparison between a received hash index based on a flow label of a data packet and the entire hash directory of network IP addresses. The CAM selects the network IP address for routing the data packet based on a match during the comparison of the received hash index and the entire hash directory of network IP addresses (See col. 3, lines 18-21 and col. 6, lines 47-49). The cited portions of Cheriton do not teach using hashing signals to enable portions of a CAM and instead teach the entire CAM being responsive to hash signals. Therefore, modifying the router disclosed by Harguchi to contain a CAM responsive to hash signals instead of destination addresses does not teaching enabling portions of the CAM in response to the hash signals, but rather the modification teaches a CAM being responsive to a different type of input signal. Accordingly, it is believed that independent claims 1, 8, 15, 22, 28, and 34 as well as dependent claims 2-7, 9-14, 16-21, 23-27, 29-33 and 35-38 are in condition for allowance.

Applicant has made a diligent effort to place the instant application in condition for allowance. Accordingly, a Notice of Allowance for pending claims 1-38 and 41-44 is respectfully requested. If the examiner is of the opinion that the instant application is in

condition for disposition other than through allowance, the examiner is respectfully requested to contact applicant's attorney at the telephone number listed below.

Respectfully submitted,

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